TITLE 400G QSFP-DD FR4 2km Transceivers	**DOC No.**	**DTRX-220809**
	REVISION：01	**AUTHORIZED BY：Albert Lin**
	DATE：2022.08.23	**CLASSIFICATION：Optical Transceiver**

1. PRODUCT FEATURES

- QSFP-DD MSA rev 5.0 compliant
- 100G Lambda MSA compliant
- 802.3cu compliant
- 400GE FR4 specification compliant
- QSFP-DD CMIS4.0 management interface compliant
- Non-hermetic package design
- 4 CWDM lanes MUX/DEMUX design
- 8 x 53.125 Gbps PAM4 electrical interface (400GAUI-8)
- Maximum power consumption 12 W
- LC duplex connector
- 425 Gbps aggregate bit rate
- Up to 2 km transmission on single mode fiber with FEC
- Single 3.3 V power supply
- RoHS 2 compliant

2. PRODUCT DESCRIPTION

2.1 PRODUCT NAME AND SERIES NUMBER(S)

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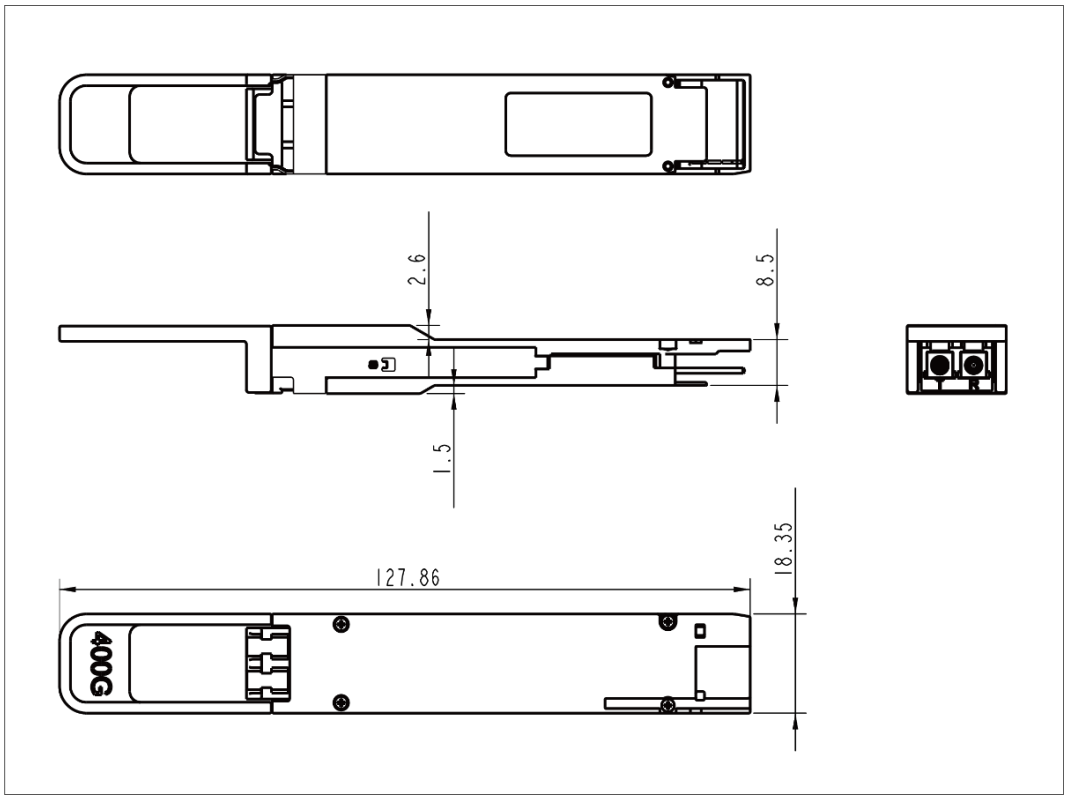
Part Number	Data Rate	Wavelength (nm)	Optical Power	Sensitivity	Connector	Temp.
P66009GGCK02-1	400G	CWDM	-3.3 ~ 3.5 dBm	-4.6 dBm	LC	**C**

2.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Unit is millimeter. All dimensions are ±0.1mm unless otherwise specified

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3. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 400G Ethernet
- Data Center Network

4. Absolute Maximum Ratings & Recommended Operating Conditions

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Maximum supply voltage	Vcc	–0.3	3.6	V
Storage temperature	Ts	–40	85	°C
Relative humidity	RH	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Type	Max.	Unit
Supply voltage	Vcc	3.135	3.3	3.465	V
Case temperature	Tc	0		70	°C
Data rate accuracy		–100		100	ppm
Link Distance		0.5		2000	m

Note: G.652 Single-mode optical fiber.

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Transmitter Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.
Data rate, each Lane	GBd	53.125 ± 100 ppm		
Modulation format		PAM4		
Line wavelengths	nm	1264.5	1271	1277.5
		1284.5	1291	1297.5
		1304.5	1311	1317.5
		1324.5	1331	1337.5
Total average launch power	dBm			9.5
Average launch power, each lane	dBm	–3.3		3.5
Optical modulation amplitude (OMA), each lane	dBm	–0.2		3.7
Extinction ratio (ER)	dB	3.5		
Side-mode suppression ratio (SMSR)	dB	30		
Launch power in OMA minus TDECQ, each lane, for ER ≥ 4.5 dB	dB	–1.7		
Launch power in OMA minus TDECQ, each lane, for ER < 4.5 dB	dBm	–1.6		
Transmitter and dispersion eye closure for PAM4, each Lane (TDECQ)	dB			3.4
Difference in launch power between any two lanes (OMA outer)	dB			4
RIN17.1OMA	dB/Hz			–136
Optical return loss tolerance	dB			17.1
Transmitter reflectance	dB			–26
Average launch power of OFF transmitter, each Lane	dBm			–20

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Receiver Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.
Data rate, each Lane	GBd	53.125 ± 100 ppm		
Modulation format		PAM4		
Line wavelengths	nm	1264.5	1271	1277.5
		1284.5	1291	1297.5
		1304.5	1311	1317.5
		1324.5	1331	1337.5
Damage threshold, each lane	dBm	4.5		
Average receiver power, each lane	dBm	–7.3		3.5
Receiver power, each lane (OMA)	dBm			3.7
Difference in receiver power between any two lanes (OMA)	dB			4.1
Receiver sensitivity (OMA outer), each lane (max)	dBm	See Note		
LOS assert	dBm	–20		
LOS de-assert	dBm			–8.6
LOS hysteresis	dB	0.5		
Receiver reflectance	dB			–26
Conditions of stressed receiver sensitivity				
Stressed eye closure for PAM4 (SECQ), lane under test	dB	0.9		.4
OMA outer of each aggressor lane	dBm		1.5	
Conditions of stressed receiver sensitivity				
BER FLOOR		1E – 6 @ –3.1 ~ 2 dBm		

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Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Notes
Power dissipation			12	W	
Supply current			3.63	A	
Receiver (module input)					
Data rate, each lane	26.5625 ± 100 ppm			GBd	
Overload differential voltage pk-pk	900			mV	
Common mode voltage	–350		2850	mV	
Differential termination resistance Mismatch			10	%	At 1 MHz
Differential return loss (SDD11)			Equation (16-1)	dB	OIF-CEI- 56G-VSR-PAM4
Common mode to differential Mode conversion (SCD11)			Equation (16-2)	dB	OIF-CEI- 56G-VSR-PAM4
Stressed input test	See OIF-CEI-56G-VSR-PAM4 Section 16.3.10.3				
Transmitter (module output)					
Data rate, each lane	26.5625 ± 100 ppm			GBd	
Differential voltage, pk-pk			900	mV	
Common mode voltage (Vcm)	-350		2850	mV	
Common mode noise, RMS			17.5	mV	
Differential termination resistance Mismatch			10	%	At 1 MHz
Differential return loss (SDD22)			Equation (16-1)	dB	
Common mode to differential Mode conversion (SCD22)			Equation (16–3)	dB	
Common mode return loss (SCC22)			–2	dB	From 250 MHz to fb GHz
Transition time	9.5			ps	
Near-end eye width at 10^{-6}	0.265			UI	

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probability (EW6)					
Near-end eye height at 10^{-6} probability (EH6)	70			mV	
Far-end eye width at 10^{-6} probability (EW6)	0.20			UI	
Far-end eye height at 10^{-6} probability (EH6)	30			mV	
Near-end eye linearity	0.85				

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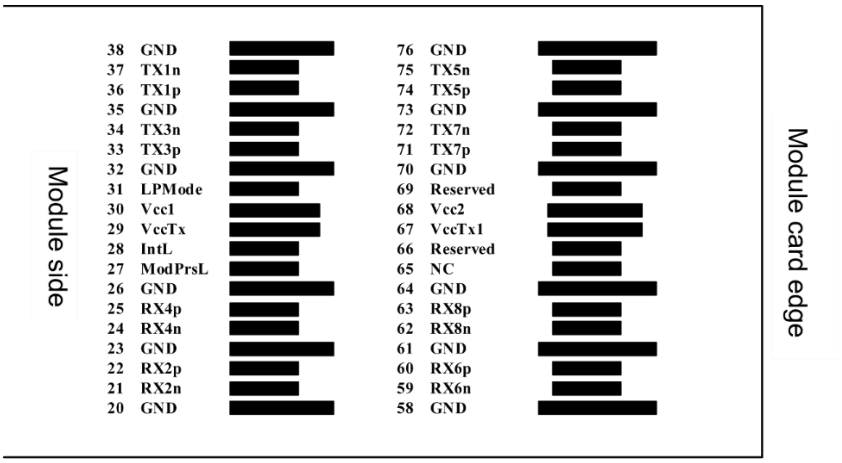
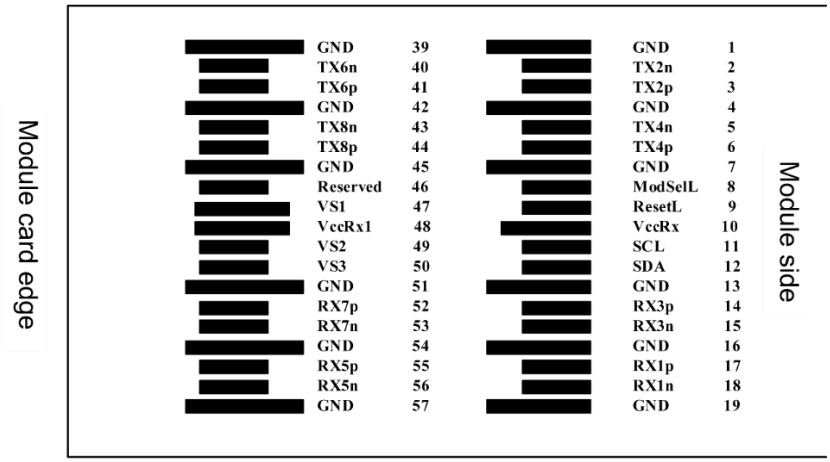
5. Applications Note:



Top side viewed from top



Bottom side viewed from bottom

Pin Definitions

Pin	Logic	Symbol	Description	Plug sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	

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3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	

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29		VccTx	+3.3 V Power Supply Transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For Future Use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3 V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1

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55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	+3.3 V Power Supply	2A	2
68		Vcc2	+3.3 V Power Supply	2A	2
69		Reserved/(ep ps)	Precision Time Protocol (PTP) Reference Clock Input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Inp ut	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of

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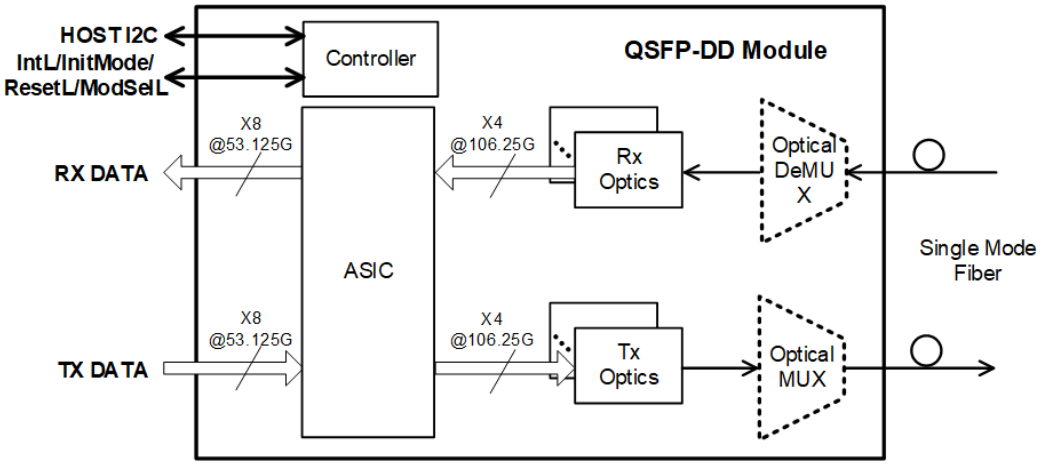
the Host Card Edge Connector are listed in the table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. *All Vendor Specific, Reserved and No Connect pins may be terminated with 50 Ω to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kΩ and less than 100 pF.*
4. *Plug Sequence specifies the mating sequence of the host connector and module.*

Figure 1-1 Transceiver block diagram



6. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2022/08/30	Albert Lin	Mike Sun